ABSTRACT

A time-sliced discrete-time Phase Locked Loop which is suitable for simultaneously synchronizing multiple input signals to multiple output signals is provided by implementing a discrete-time phase detector, loop filter, and voltage controlled oscillator that together operate as a single discrete-time PLL in hardware and applying control logic to retrieve the history for each signal pair from a context memory (RAM), to enable the discrete-time PLL hardware, and to store the resulting history in the context memory for use in subsequent operations for a particular input/output signal pair.